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DESIGN AND IMPLEMENTATION OF VEDIC MULTIPLIER ON SPARTAN-6 FPGA USING VERILOG HDL

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ABSTRACT

Vedic Mathematics can rapidly conduct a several arithmetic operations. The multiplier unit is an essential part of general purpose and digital signal processors that greatly influences the processing speed. The Urdhva-Tiryagbhyam, a technique from Vedic math that makes it simple to multiply given integers as well, is utilized in this study to initiate a high-speed multiplier architecture. To determine product of two numbers, utilize the vertical and crosswise approaches referred to as Urdhva-Tiryagbhyam. Applying traditional Vedic mathematics, the paper discusses the creation of 2x2, 4x4, 8x8, 16x16, and 32x32 bit Vedic multipliers. The multipliers were synthesized and simulated using XILINX ISE Design Suite v.14.7 software. The multipliers were generated and defined using Verilog Hardware Description Language (VHDL).

KEYWORDS

Vedic Mathematics, Urdhva-Tiryagbhyam, Verilog, FPGA

1. INTRODUCTION

A multiplication method named the Vedic multiplier was created in ancient Indian mathematics, particularly the Vedic scientific framework. The Vedic multiplier is one of the techniques used in Vedic arithmetic, which may be a collection of techniques and methods to perform quick mental calculations. In terms of actual applications, highly optimized duplicate calculations, like binary multiplication using hardware circuits, are used by sophisticated computerized frameworks and computers. [1] An arithmetic circuit or calculation that achieves duplication, particularly with binary integers, is known to be a binary multiplier. It receives two binary digits, frequently called the multiplicand and multiplier, and outputs their item. The majority of processes involve calculating several partial products, and then adding the results together. Although modified here, this procedure still performs lengthy multiplication on the base-tenth integrability but in this case, has been altered for usage with a binary number system. Instead of utilizing one adder to process each partial product, it began to be feasible to fit enough adders on just one chip to total all of the partial outcomes at once. Individually as more transistors per chip became possible as a result of large-scale integration. Instead of using it became feasible to fit enough adders on one chip to

complete all the partial products concurrently, as opposed to using a single adder for processing each part of the product independently. We may simulate and synthesize the design to get a digital circuit that performs multiplication using the Vedic approach by using the Vedic multiplier in Verilog HDL. When multiplication operations are necessary, this circuit can be integrated into bigger systems, such as processors or digital signal processing applications. It is significant to point out that additional efficiency and performance advancements can be made to the Verilog Vedic multiplier implementation through optimization like parallelism, pipelining, and the use of specialized hardware components like carry-save adders. Overall, the Vedic multiplier implementation in Verilog HDL provides a way to integrate classical mathematical techniques into modern digital systems and investigate different multiplication methods [1-65].

2. VEDIC MATHEMATICS

Carl Friedrich Gauss once said that mathematics is the "Queen of the Sciences." All sciences have their roots in math, which also serves as their foundation. The Veda is the source of Vedic mathematics, which offers a one-line, Very quick cross-checking, and issue resolution are both priorities [5]. The word "Veda," which originates from the Sanskrit word Vid and meaning "to know without limit," refers to all of the Veda-sakhas that are known to humankind. The Veda is a storehouse of all knowledge and, as one delves deeper into it, becomes more and more insightful. The idea of Vedic mathematics was reintroduced to this world by Sri Bharati Krishna Tirthaji. He created sixteen straightforward mathematical formulas known as thirteen sutras Corollaries or up-sutras after studying the Atharva Veda in depth. The sutras' system is particularly straightforward and effective because it encompasses practically all areas of mathematics. The Sutras' application is entirely logical and sensible, even though it appears to be magic when arithmetic problems can be solved in one line faster. The sixteen sutras may efficiently do all basic operations, including subtraction, multiplication, addition, and division for any processor. In this case, we've used a multiplication method called Urdhva Tiryagbhyam. The 16 sutras, which assign a set of characteristics to a number or a collection of numerals, are the foundation of Vedic mathematics. In 16 Sutras (Phrases) and 120 phrases, the prehistoric Hindu mathematicians (Rishis) of Bharat outlined straightforward procedures for resolving all mathematical issues in two or three simple steps. In comparison to nowadays math, Vedic math helps a person solve math issues more quickly. Vedic math training has been discovered to help pupils solve difficult or simple mathematical issues by helping them make wise decisions and stay away from stupid mistakes. Vedic mathematics has been demonstrated to increase attention and decrease memory levels, allowing pupils to learn and improve their skills. It helps to improve logical thinking abilities and acquire a better comprehension of both fundamental and complex mathematical subjects. Crosswise is the most widely employed way in Urdhva Tiryagbhyam, which means vertically. [8] Urdhva Tiryagbhyam is applicable in all situations and can be applied to multiplying decimal and binary integers. The Urdhva Tiryakbhyam sutra's methods for multiplying two decimal integers illustrate the method in Fig. 1. The numbers at the end of the queue are multiplied, likewise, if a prior carry is present, It's also included. Any step that has been multiplied more than once is added to the preceding carry as well. The phrase "carry" for the following step is the tens place digit, while the term "result bit" refers to the unit place digit. Because sums and partial products are computed concurrently, processor clock frequency has no bearing on the multiplier. Microprocessors do not have to run at an ever-increasing frequency as a result, which maximizes their processing power. Its uniform structure makes it simple to arrange in a silicon chip. As a result, it is a technique that saves time, energy, and space as compared to multiplication in the classic sense.

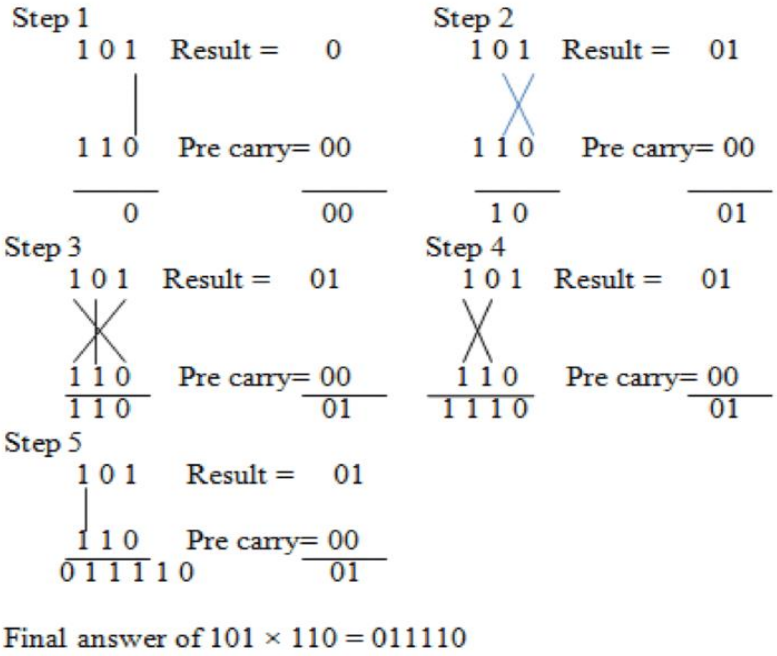


Figure 1. Multiplication of two binary number using Urdhva-Triyagbhyam sutra[1]

3. VLSI DESIGNS USING VEDIC MATHEMATICS

3.1. Vedic Multiplier for 2x2 bit

Figure 2 illustrates a 2x2-bit block diagram. [3] For a 2x2 bit Vedic multiplier, where b and a are input variables and a has input a0 and a1 and b has input b0 and b1, the first bit of output is found by multiplying a0 and b0, the second bit is created by adding the multiplication of b0, a1 and b1, a0, and the third bit is found by combining the carry from the previous operation with the multiplication of a1, b1 and the final bit is established by applying the carry discovered during the last summation process. Here, we have used 2 half-adders and a gate.

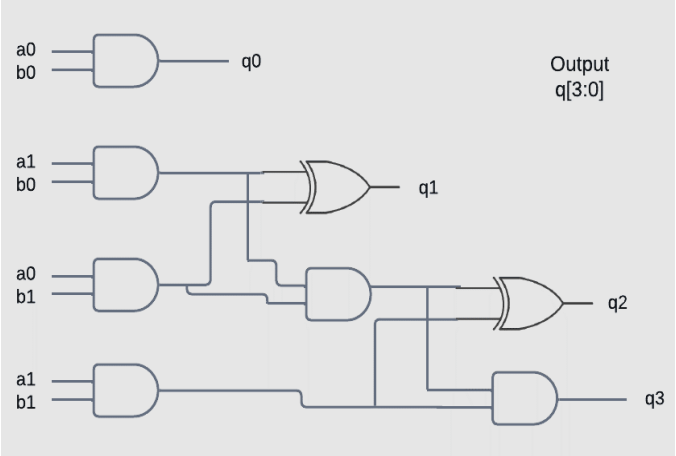


Figure 2: 2x2 bit block diagram [2]

As illustrated in figure 3: Result of a 2x2 bit Vedic Multiplier, where b and a are the inputs and c is the four-bit output. So, at initially, both inputs are zero, so the output is also zero; then, if the input for a is 01 and the input for b is 11, the output is 0011. Similarly, if a's input is 10 and b's input is 11, the output will be 0110.

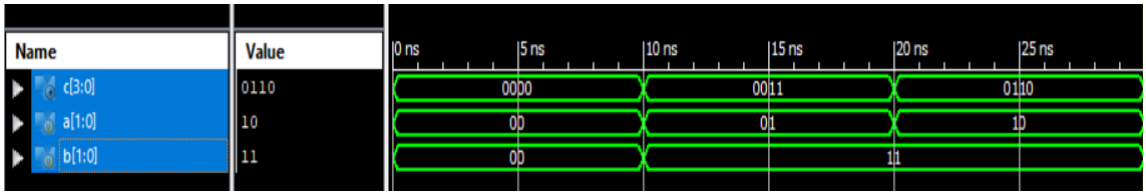


Figure 3: Simulation result of Vedic Multiplier for 2x2 bit

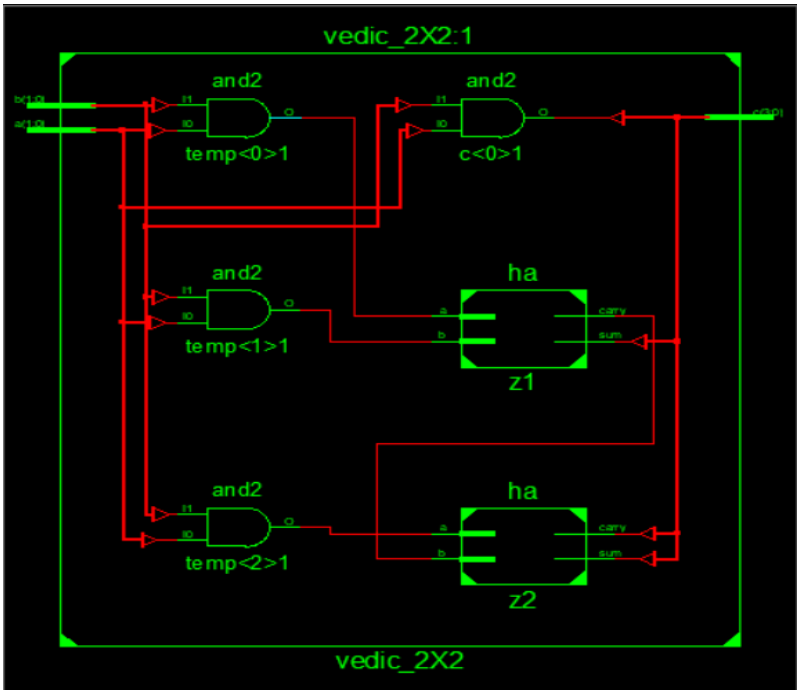


Figure 4: RTL Schematic of 2x2 bit Vedic Multiplier

3.2. Vedic Multiplier for 4x4 bit

The suggested Vedic multiplier can be applied to shorten waiting times. Vedic multipliers with array multiplier structures are mentioned in early literature. [3] The configuration of Adders in Fig. 5 enables us to shorten the delay. It's interesting to note that the 4x4 Vedic multiplier module can have four Vedic multiplier modules of size 2x2. The final result is created by adding the outputs of 2x2 bit multipliers. The multiplier calculates the partial products and adds them using a 2x2-bit Vedic multiplier and adders before performing a 4x4-bit multiplication. Sections of the multiplication operation are performed, and the different outputs are combined and summed to get the final outcome. Here, a total of two 6-bit adders and one 4-bit adder are needed.

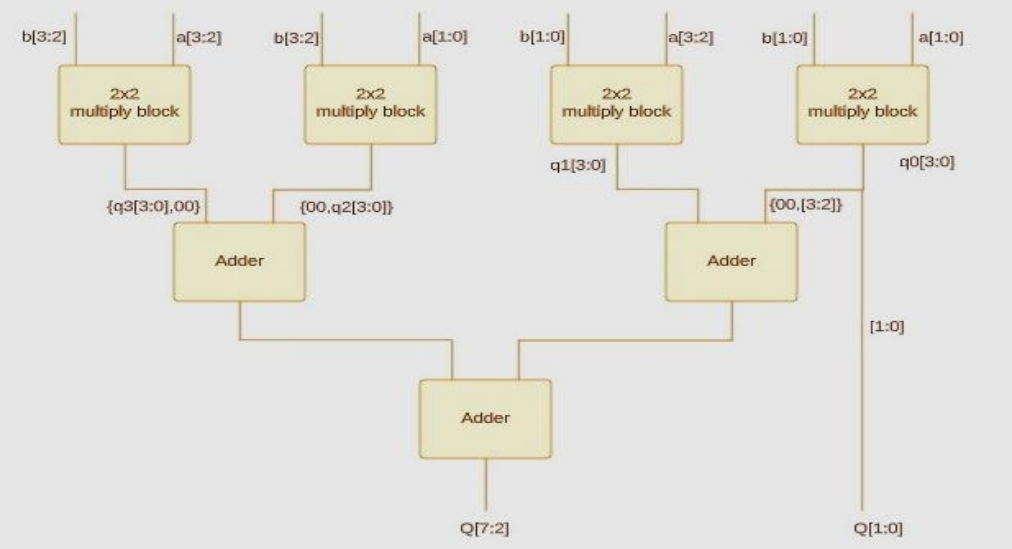


Figure 5: 4x4 bit block diagram [2]

As shown in fig 6: Result of a 4x4 bit Vedic Multiplier, where b and a are the inputs and c is the eight bit output. So, if the input for a is 0101 and the input for b is 1010, the output is 00110010. Similarly, if a's input is 1101 and b's input is 0100, the output will be 0110100. Figure 6: Simulation result of Vedic Multiplier for 4x4 bit

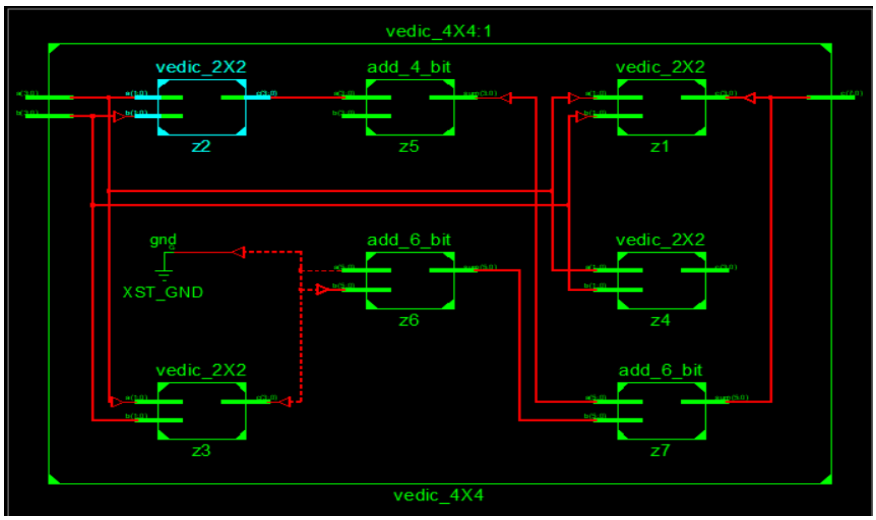


Figure 7: RTL Schematic of 4x4 bit Vedic Multiplier

We also implemented it on the Spartan 6 FPGA board. Here, we have used the FPGA board's input and output lines to provide the first and second inputs, respectively 1010 and 1110, and we are receiving an 8-bit output of 10001100.

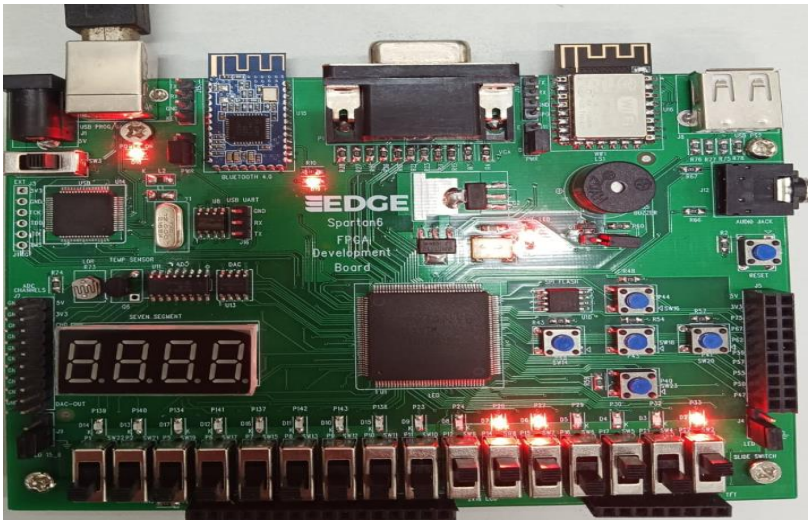


Figure 8: FPGA Implementation of 4x4 bit Vedic Multiplier

3.3. Vedic Multiplier for 8x8 bit

We used four Vedic Multiplier modules of 4x4 bit to create a Vedic Multiplier of 8x8 bit. As illustrated in Figure 9, a is divided into two halves, ah and al, while b is divided into two halves, bh and bl. As a result, combinations such as ahbh, bhal, blah, and albl are possible. This combination will be processed through a Vedic multiplier of 4x4 bit, and the output of the four Vedic multipliers will be passed via adders before arriving at a 16-bit output. The multiplier calculates the partial products and adds them using 4x4-bit Vedic multipliers and adders, which results in an 8x8-bit multiplication. The multiplying operation is broken down into stages, and the interim results are combined and added to get the end result.

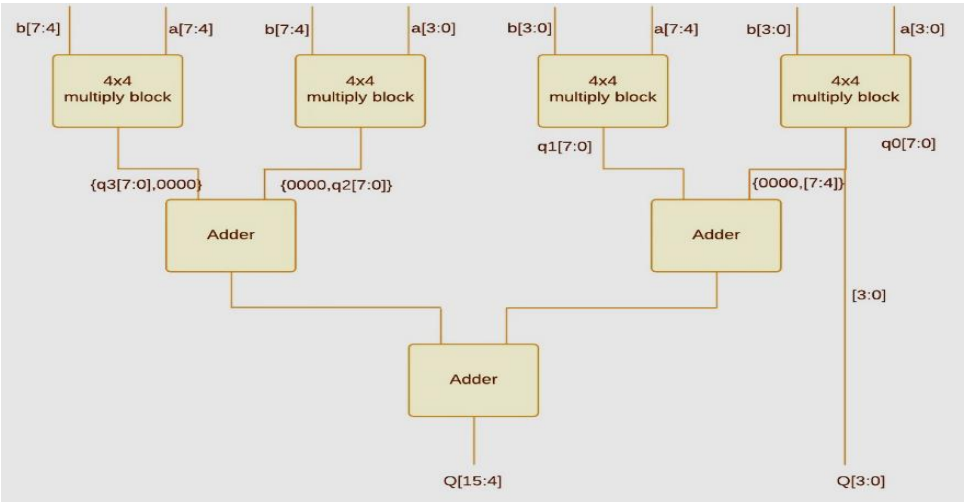


Figure 9: 8x8 bit block diagram [2]

As shown in fig 10: Result of 8x8 bit Vedic Multiplier, where a and b are the inputs and c is the sixteen-bit output. So, if the input for a is 01010101 and the input for b is 10101010, the output is 0011100001110010. Similarly, if a's input is 01100111 and b's input is 11010100, the output will be 0101010101001100.

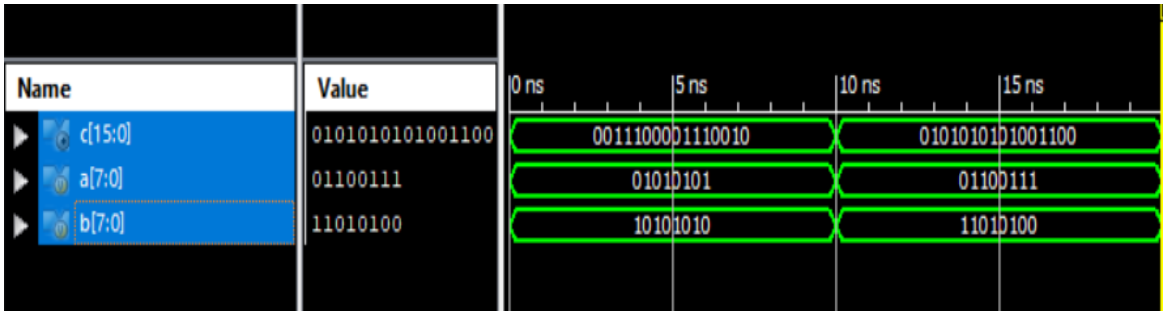


Figure 10: Simulation result of Vedic Multiplier for 8x8 bit

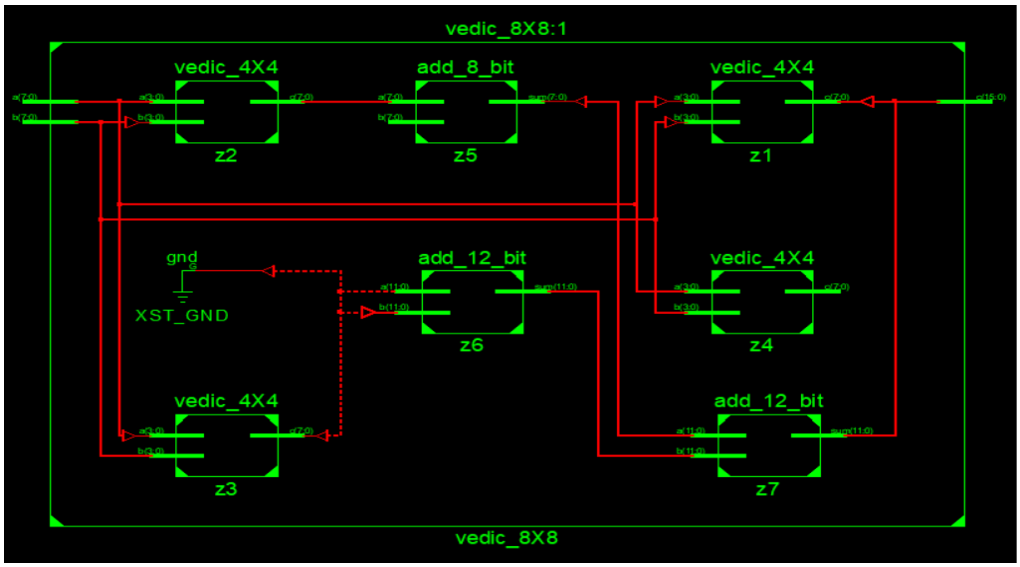


Figure 11: RTL Schematic of 8x8 bit Vedic Multiplier

We also implemented it on the Spartan 6 FPGA board. Here, we have provided the first and second inputs of 8-bit from input and output lines of the FPGA board, respectively, and are receiving the 16-bit output. The first and second both inputs are 11111111 and the output we have received is 1111111000000001.

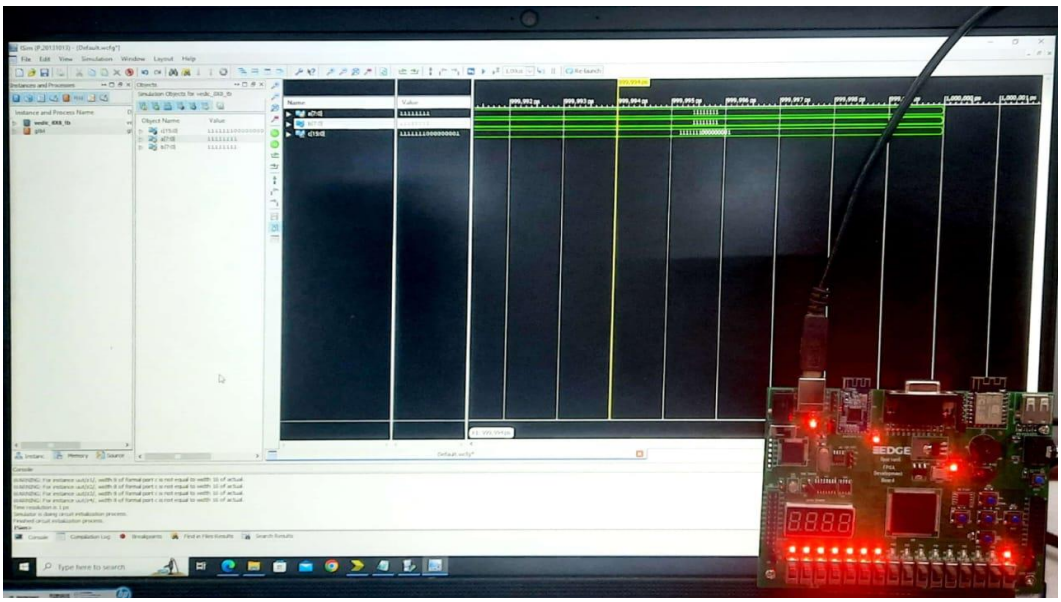


Figure 12: FPGA Implementation of 8x8 bit Vedic Multiplier

3.4. Vedic Multiplier for 16x16 bit

The multiplication utilizes the four-bit multiplier block to accomplish the fundamentals of Vedic multiplication, which have been discussed. The final result is created by adding the outputs of 8x8 bit multipliers. In order to determine the partial products and add everything together, the multiplier conducts a 16x16 multiplication using 8x8-bit Vedic multipliers and adders. The multiplication procedure is broken down into steps, and the intermediate outputs are combined and summed to produce the final output. As indicated in Figure. 13, a total of three adders—two 12-bit, and one 8 bit—are needed.

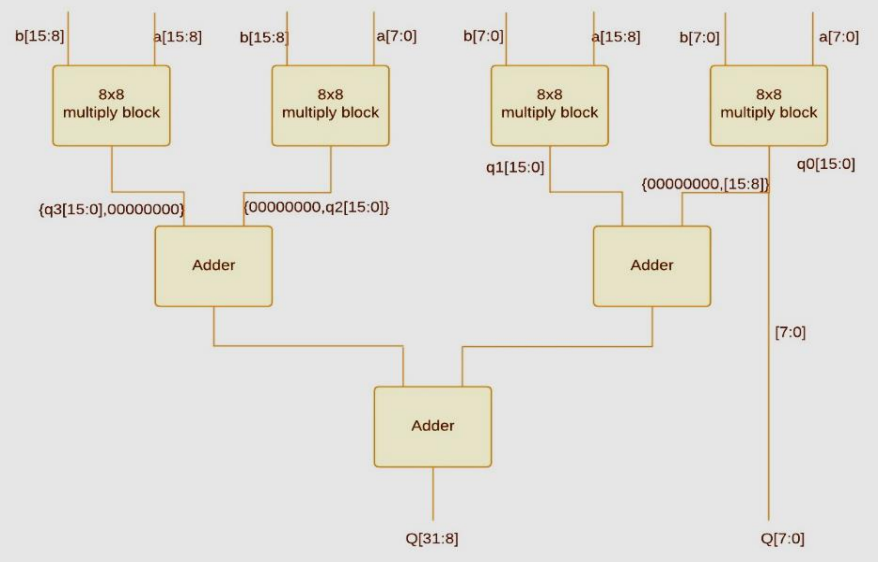


Figure 13: 16x16 bit block diagram [2]

As shown in fig 14: Result of 16x16 bit Vedic Multiplier, where b and a are the inputs and c is the 32-bit output. So, if the input for a is 1010101010101010 and the input for b is 0000111100001111, the output is 00001010000010011111010111110110. Similarly, if a's input is 0101010101010101 and b's input is 1111000011110000, the output will be 01010000010011111010111110110000. Figure 14: Simulation result of Vedic Multiplier for 16x16 bit

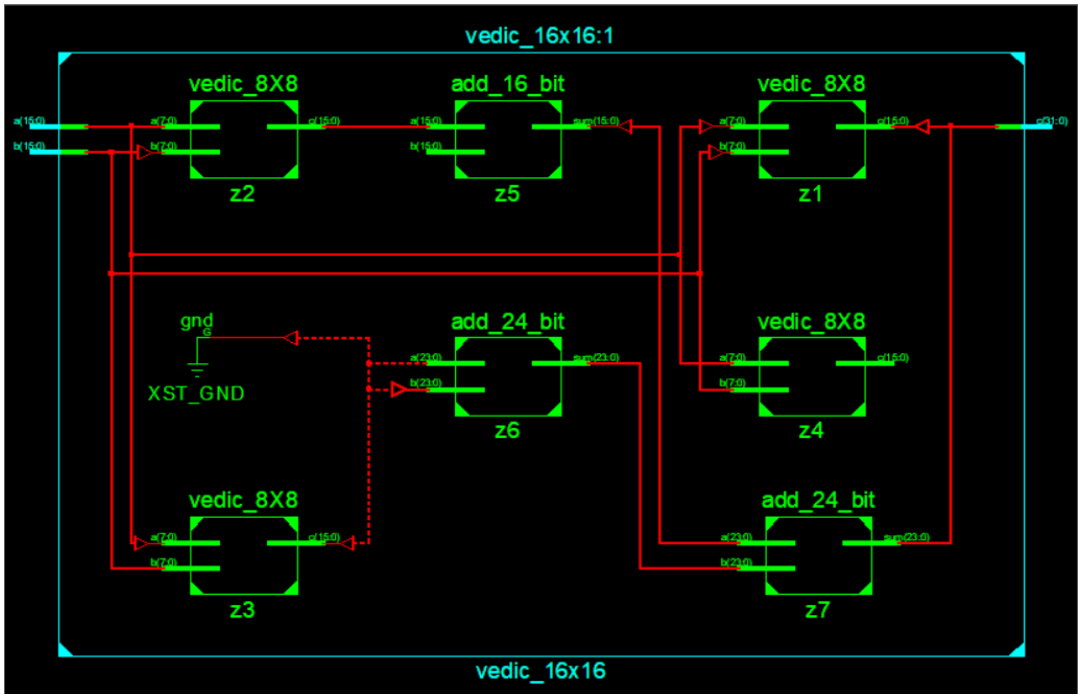


Figure 15: RTL Schematic of 16x16 bit Vedic Multiplier

3.5. Vedic Multiplier for 32x32 bit

Four 16x16 Vedic multiplier modules can simply create a Vedic multiplier module for 32x32 bits. To create the final output, the outputs of multipliers of 16x16 bit are passed through adders in the appropriate order. The Vedic multiplication accomplishes efficient and feasible multiplication for big operands by segmenting the result of multiplication into smaller parts and effectively combining the partial results using adders. As indicated in Figure. 16, a total of two 48-bit and one 32-bit adders are needed.

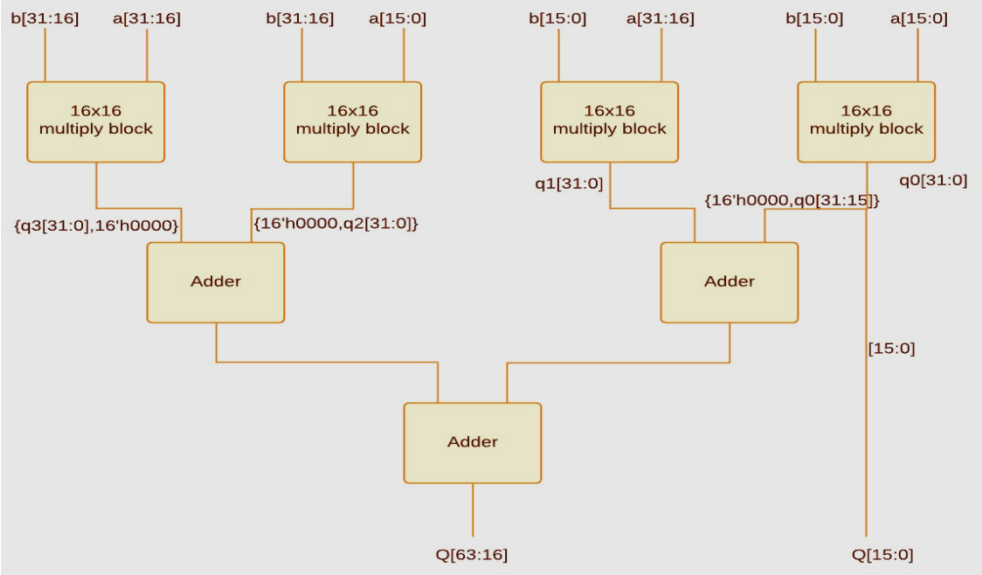


Figure 16. 32x32 bit block diagram [2]

As shown in Figure 17: Result of 32x32 bit Vedic Multiplier, where a and b are the inputs and c is the 32-bit output. So, if the input for a is 32'h12345000 and the input for b is 32'h00001234, the output is 64'h0000014b60404000.

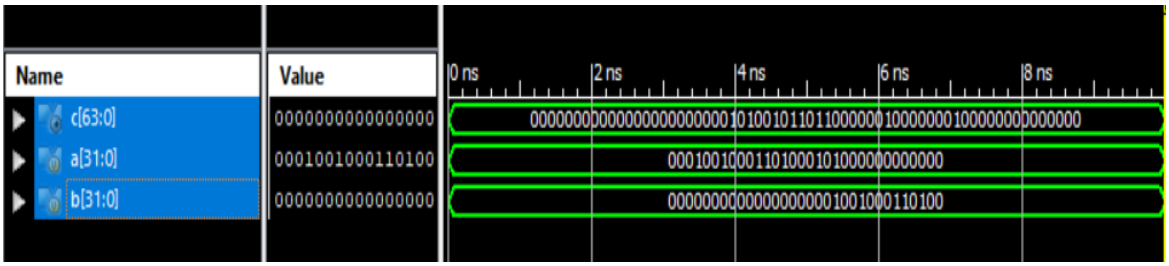


Fig 17: Simulation result of Vedic Multiplier for 32x32 bit

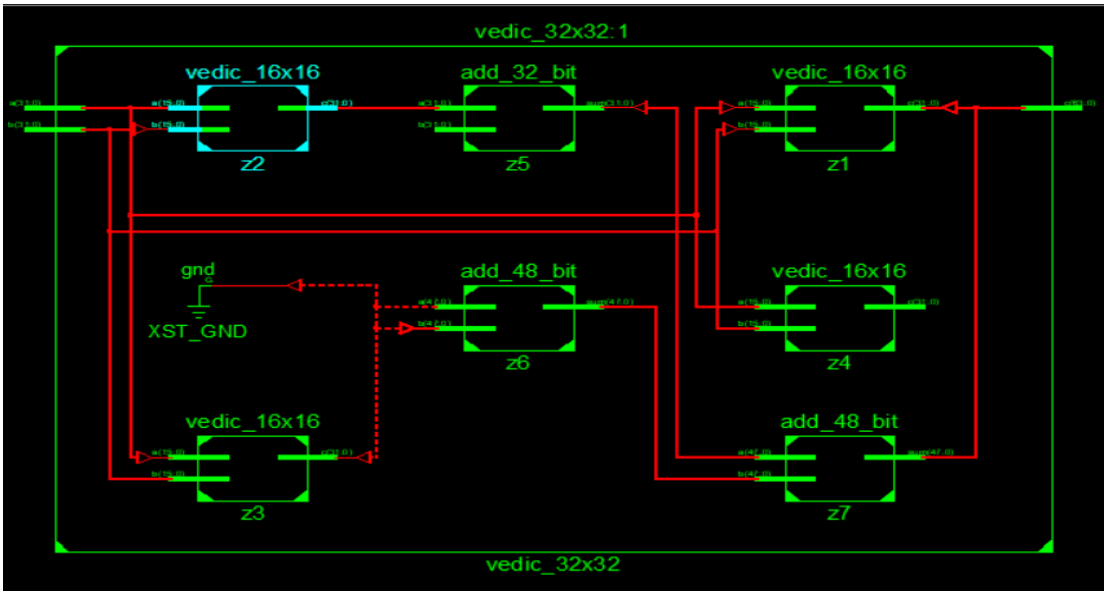
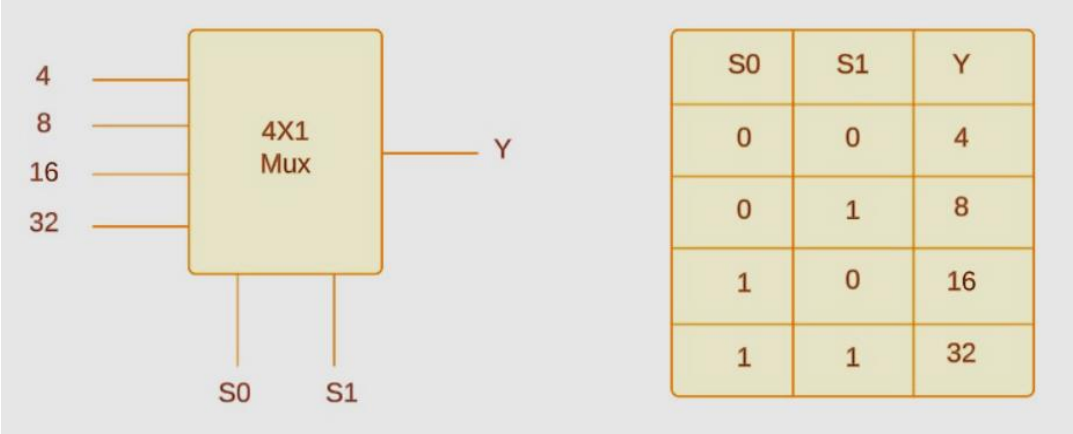


Fig 18: RTL Schematic of 32x32 bit Vedic Multiplier

4. VEDIC MULTIPLIER USING 4X1 MUX FOR VARIABLE INPUTS BITS

We have created a Verilog code for the Vedic multiplier using 4x1 mux. There are therefore 4 inputs and 2 selection lines, and each selection line determines which input is sent on to the output. [10] As inputs, we have provided four different modules: the first input module is a 4x4 bit module, the second is an 8x8 bit module, the third is a 16x16 bit module, and the fourth is a 32x32 bit module. As depicted in Fig. 19, inputs will be called based on the selection lines. For example, if both S0 and S1 are zero, the module for 4x4 bits will be sent to the output, if S0 is 0 and S1 is 1 then the module for 8x8 bits will be sent to the output, the module for 16x16 bits will be sent to output when S0 is 1 and S1 is 0 and the module for 32x32 bits will be sent to output if S0 and S1 are both 1. This Vedic multiplier can handle up to 4 inputs of any number of bits; if we need to add more inputs, we can use a larger mux.



S0	S1	Y
0	0	4
0	1	8
1	0	16
1	1	32

Fig 19: 4X1 Block Diagram

As shown in figure 20: Result of Vedic Multiplier, where d,c,b,a and sel are the inputs and out is the output. So, if the input for sel is 00 then module 4x4 is called and inputs a and b are used. Similarly, if sel is 01, 10, 11 then it will call module 8x8 which will use b and c inputs, 16x16 in which c and d inputs are used and 32x32 which has d as inputs respectively.

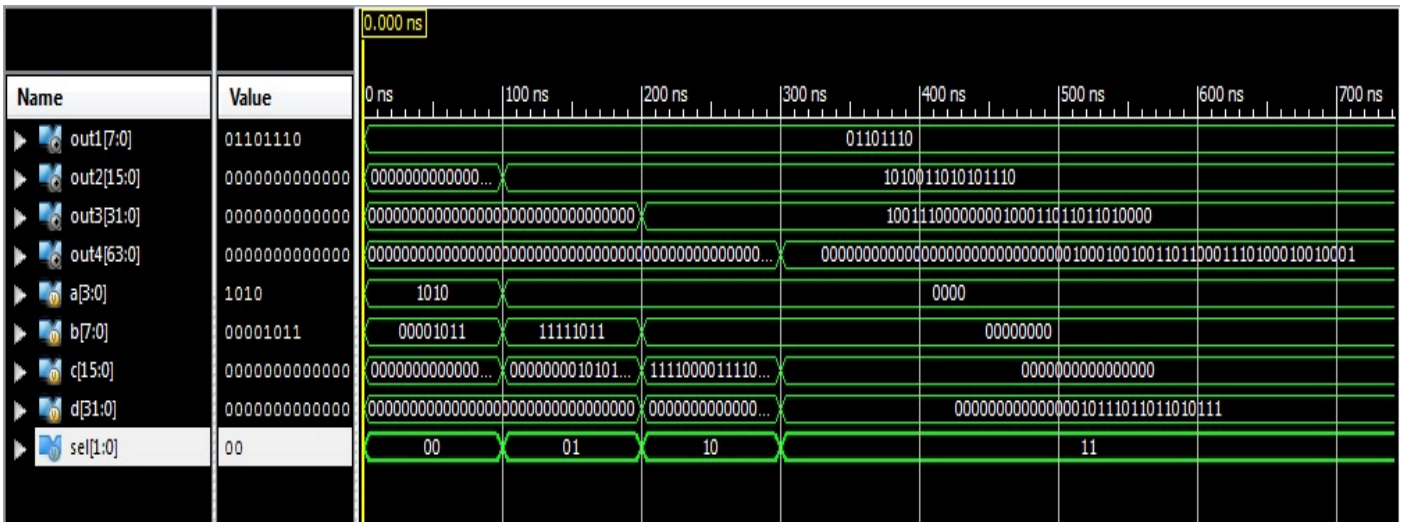


Fig 20: Simulation result of Vedic Multiplier using 4x1 mux

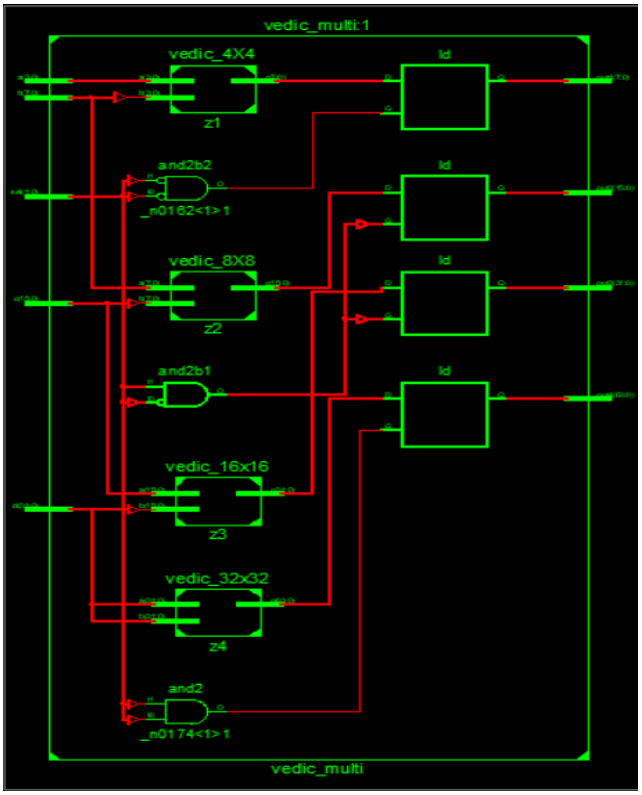


Fig 21: RTL Schematic of Vedic Multiplier using 4x1 mux

5. ADVANTAGES

The key advantage of the Vedic multiplier is that it is faster than other multipliers because as the bit size grows, the area and delay grow gradually. For the previously mentioned 8x8, 16x16, etc. multipliers, the Vedic multiplier requires fewer gates, which results in extremely little power dissipation and minimal power consumption. Another benefit is in comparison to other multipliers, gate latency and area rise extremely gradually as the total amount of bits increases. The number of components used in the Vedic multiplier is reduced. As a result, it saves time and space. It provides the fastest speed of any conventional multiplier, as well as better throughput operations. When compared to other multipliers, the Vedic multiplier offers the largest benefit in terms of gate delays and structure regularity.

6. DISADVANTAGES

When there are high numbers, the system experiences carry propagation delay because of Urdhva-Tiryakbhyam architecture. Another drawback is that the propagation time in computing the RHS portion of the method also dramatically increases when the total amount of bits grows over 32 or 64 bits. Even the system itself gets complex when multiplying complex numbers.

7. APPLICATION

The rate of multiplication processes is critical in DSP. A form of technology called digital signal processing is used in almost all technical fields. It additionally represents the field of expertise that has advanced the fastest in the past ten years., posing enormous difficulties to the technical

sector. Rapid multiplication and addition processes are critical in DSP for Convolution, DFT, and Digital filters. It is utilized in the design of low-powered VLSI devices. It is also employed in frequency domain filtering (FIR and IIR), correlation, and digital image processing. Due to the fact that the great Vedic multiplication is quick, ALU employs this technique to provide consistent output. It is also used in real time signal.

8. CONCLUSION

The Vedic multiplier is one of the techniques used in Vedic arithmetic, which may be a collection of techniques and methods to perform quick mental calculations. In addition to enhancing accuracy, the goal of boosting speed and to decrease time, power, and processing latency. In Vedic mathematics, there are a total of 16 sutras, and we have used Urdhva Tiryagbhyam sutra, which means across and vertical from which we have created different modules of different bits for Vedic Multiplier. This paper shows Vedic Multipliers for various bits such as 2x2, 4x4, 8x8, 16x16, 32x32, and a Vedic Multiplier that is produced using a 4x1 mux utilizing a Verilog HDL that is only applicable to 4 inputs. Moreover, we implemented the 4x4 bit and 8x8 bit Vedic multipliers on the Spartan 6 FPGA board.

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